

## DESIGN FOR MANUFACTURABILITY AND YIELD FOR NANO SCALE CMOS%0A

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DESIGN FOR MANUFACTURABILITY AND YIELD FOR NANO-SCALE CMOS

DESIGN FOR MANUFACTURABILITY AND YIELD FOR NANO-SCALE CMOS by CHARLES C. CHIANG Synopsys Inc, Mountain View, CA, USA and JAMIL KAWA Synopsys Inc, Mountain View, CA, USA

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This book walks the reader through all the aspects of manufacturability and yield in a nano-CMOS process. It covers all CAD/CAE aspects of a SOC design flow and addresses a new topic (DFM/DFY) critical at 90 nm and beyond.

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Design for Manufacturability and Yield for Nano-Scale CMOS walks the reader through all the aspects of manufacturability and yield in a nano-CMOS process and

how to address each aspect at the proper design step starting with the design and layout of standard cells and how to yield-grade libraries for critical area and lithography artifacts through place and route, CMP model based simulation

#### **Design for Manufacturability and Yield for Nano-Scale CMOS**

Yield and manufacturability have to be designed in, and they are everybody's responsibility. Design for Manufacturability and Yield for Nano-Scale CMOS walks the reader through all the aspects of manufacturability and yield in a nano-CMOS process and how to address each aspect at the proper design step starting with the design and layout of standard cells and how to yield-grade libraries for

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Manfred Dietrich , Uwe Eichler , Joachim Haase, Digital statistical analysis using VHDL: impact of variations on timing and power using gate-level Monte Carlo simulation, Proceedings of the Conference on Design, Automation and Test in Europe, March 08-12, 2010, Dresden, Germany